

AMENDMENTS TO THE DRAWINGS

Please replace drawing sheets 1-49 with the replacement sheets attached hereto.

REMARKS**Status of the Claims**

Claims 1-30 are currently present in the Application, and claims 1, 11, and 21 are independent claims. Claims 1, 4-7, 9, 11, 14-17, 19-27, 29, and 30 have been amended in this Response. Applicants are not conceding in this Application that those claims are not patentable over the art cited by the Examiner, as the present claim amendments are only for facilitating expeditious prosecution of the Application. Applicants respectfully reserve the right to pursue these and other claims in one or more continuation and/or divisional patent applications.

In particular, Applicants have amended independent claim 1 to include limitations previously found in dependent claim 7. Similarly, Applicants have amended independent claims 11 and 21 to include limitations previously found in dependent claims 17 and 27, respectively. Further support for these amendments is found in Applicants' specification on page 47, line 25 through page 50, line 16 (also see Figures 43 and 44). No new matter has been added as a result of these amendments.

Applicants have further amended independent claim 21 to clarify that Applicants claim a computer program product stored on a computer operable media, the computer operable media containing instructions for execution by a computer, which, when executed by the computer, cause the computer to perform the claimed method. Claims 22-27, 29, and 30 have been amended to be consistent with independent claim 21. Support for these amendments is found in Applicants' specification on page 60, line 16 through page 61, line 3. No new matter has been added as a result of these amendments.

Information Disclosure Statements

Applicants note that Information Disclosure Statements (IDSs) were filed on January 4, 2007, October 13, 2006, and September 19, 2006. Each IDS included a Form PTO-1449. However, the initialed copies of these forms have not been returned to Applicants. Applicants respectfully request that the IDSs be considered, and the

initiated Forms PTO-1449 be returned with the next action. Copies of the filed IDSs, Forms PTO-1449, and EFS-Web receipts are attached hereto.

Drawings

The drawings are objected to as they appear to have been scanned into the system out of alignment. Applicants hereby resubmit the drawings, as requested by the Examiner, and therefore respectfully request that the Examiner remove the objections to the drawings.

Claim Objections Under 35 U.S.C. § 112

Claims 4, 9, 14, 19, 24, and 29 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended the wording of these claims as suggested by the Examiner, and therefore respectfully request that the Examiner remove the rejections under 35 U.S.C. § 112.

Claim Rejections – Alleged Obviousness Under 35 U.S.C. § 103

Claims 1-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mochizuki, U.S. Patent No. 5,490,278 (hereinafter Mochizuki) in view of Nakanishi, U.S. Patent No. 5,887,186 (hereinafter Nakanishi). Applicants respectfully traverse the rejections under 35 U.S.C. § 103.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). (Manual of Patent Examining Procedure § 2143.03). Applicants respectfully submit that claims 1-30 are patentable over Mochizuki in view of Nakanishi, as neither Mochizuki nor Nakanishi teaches or suggests all the claim

limitations of Applicants' claims. Using independent claim 1 as an exemplary claim, Applicants teach and claim the following:

- loading, at a second processor, a virtual machine program into a local memory corresponding to the second processor;
- receiving, at the second processor, a code processing request requested by a first processor, wherein the first and second processors are heterogeneous processors within a computer system that share a common memory;
- reading, from the common memory shared by the first and second processors, software code data corresponding to the request, the software code data including virtual machine code adapted to be processed by the virtual machine program;
- writing the software code data corresponding to the request to the local memory corresponding to the second processor in response to the request;
- processing the software code data by the second processor, wherein the processing includes processing the virtual machine code at the second processor using the virtual machine program, the processing resulting in executable instructions;
- writing the executable instructions to a memory location accessible by the first processor; and
- executing, at the first processor, the executable instructions.

As an initial matter, neither Mochizuki nor Nakanishi appears to teach or suggest heterogeneous processors, as taught and claimed by Applicants. Mochizuki purports to

teach using parallel processing to solve linear equations (see Mochizuki, Abstract). Although Mochizuki discusses the use of preprocessing sections, an updating section, and a back-substitution section (Mochizuki, col. 2, line 32 through col. 3, line 24), there is no indication that these sections include heterogeneous processors. The Office Action cites Mochizuki at Figure 1, reference numeral 1, as teaching heterogeneous processors (Office Action, page 3), however, reference numeral 1 points to a memory and not to a processor. Nakanishi purports to teach the use of a memory-distributed parallel processor to solve linear equations (see Nakanishi, Abstract). However, the processors in Nakanishi do not appear to be heterogeneous processors (Nakanishi, col. 2, lines 1-10). Because neither Mochizuki nor Nakanishi disclose the use of heterogeneous processor, neither Mochizuki nor Nakanishi teaches or suggests "receiving, at the second processor, a code processing request requested by a first processor, ***wherein the first and second processors are heterogeneous processors*** within a computer system that share a common memory," as taught and claimed by Applicants in independent claims 1, 11, and 21.

Applicants further submit that none of the cited art teaches or suggests "loading, at a second processor, ***a virtual machine program*** into a local memory corresponding to the second processor," and then "processing the software code data by the second processor, wherein the processing includes ***processing the virtual machine code at the second processor using the virtual machine program***, the processing resulting in executable instructions," as taught and claimed by Applicants. A close reading of both Mochizuki and Nakanishi shows no mention of a virtual machine. As known to those skilled in the art, a virtual machine engine is designed and written for a particular processor, hardware platform, and/or operating system (see Applicants' specification on page 2, line 27 through page 3, line 10 and also on page 48, lines 4-15). An application program written for a particular virtual machine, such as a Java Virtual Machine (JVM), can be run on various platforms, so long as it is run using an interpreter or is compiled for the particular platform before being run.

Applicants teach and claim that a virtual machine program is loaded into the second processor's local memory. The software code data is then processed by the second processor using the virtual machine program. This processing results in executable instructions that are then written to a memory location accessible by the first processor and executed by the first processor. Neither Mochizuki nor Nakanishi teaches or suggests any of these elements of Applicants' independent claims. The Office Action does not cite any specific portions of Mochizuki or Nakanishi as teaching or suggesting these claim elements. And, as noted above, upon a careful reading of both Mochizuki and Nakanishi, Applicants do not find any reference to a virtual machine. Therefore, Applicants respectfully submit that neither Mochizuki nor Nakanishi nor a combination of the two teaches or suggests "loading, at a second processor, **a virtual machine program** into a local memory corresponding to the second processor," and then "processing the software code data by the second processor, wherein the processing includes processing the virtual machine code at the second processor **using the virtual machine program**, the processing resulting in executable instructions," as taught and claimed by Applicants.

For the reasons set forth above, Applicants respectfully submit that independent claims 1, 11, and 21, and the claims which depend from them, are patentable over Mochizuki in view of Nakanishi, and respectfully request that they be allowed.

Notwithstanding the patentability of claims 4-6, 14-16, and 24-26 based on the above discussion, Applicants would like to further address these claims. Claims 4, 14, and 24 add elements including:

- running a first program;
- in response to running the first program, identifying a call to a software effect corresponding to the software code data; and
- loading the software code data into the common memory, wherein the processing of the software code data occurs during the running of the first

program and wherein the processing is completed prior to the first program calling the software effect.

Claims 5, 6, 15, 16, 25, and 26 add further elements having to do with multimedia effects. Neither Mochizuki nor Nakanishi includes any discussion regarding calling software effects, such as multimedia effects. As noted above, Mochizuki and Nakanishi disclose methods for solving linear equations, and do not appear to have anything to do with software effects, and in particular with multimedia effects. Therefore, Applicants respectfully submit that claims 4-6, 14-16, and 24-26 are patentable over Mochizuki in view of Nakanishi.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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